

Inside this issue:

Page 2

- Schroff's Interscale M Demonstration

Page 3

- Staff Introduction - Jonathan Knoblauch

Page 4

- Webinar by RTI—Architecting Radar Systems
- OpenCL Developer's Bundle from BittWare

Page 5

- UEI's new MIL-DNx Series
- 4DSP announces new FMC170

Page 6

- BittWare's TeraBox High Performance Reconfigurable Platform

Page 7

- WindRiver's Accelerated Safety Certification for Multi-core
- ATP's advancedMLC for embedded modules

Page 8

- AdaCore's CodePeer earns qualification for software verification in Avionics and Railway



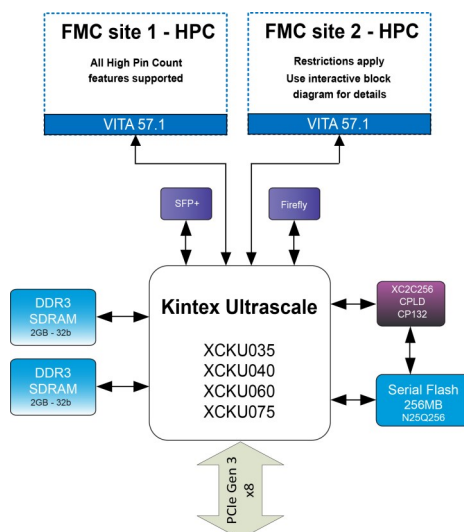
4DSP Brings Xilinx UltraScale FPGA Performance and Two VITA 57.1 FMC Sites to PCIe with the PC820

4DSP announced the release of the PC820, a high-performance PCI Express (PCIe) card with advanced Digital Signal Processing (DSP) capabilities and multiple I/O options. The card offers eight lanes of PCIe Gen 3 and up to two FMC (FPGA Mezzanine Card - VITA 57.1) sites that are closely coupled to the onboard Kintex UltraScale FPGA and 4GB of DDR3 SDRAM. The PC820 also has two serial peripheral interfaces: a single-lane SFP+ module and a dual-lane Samtec FireFly connector. The card is the newest addition to 4DSP's family of modules with high-end FPGA devices and FMC functionality in popular board form factors.



The PC820 is designed for software defined radio (SDR), RADAR/SONAR imaging, data center high-speed communication, and analog/digital signal processing among other uses. The card is an excellent choice for demanding applications that require large band signal digitisation or generation through the use of accelerated frequency-domain algorithms.

"The PC820 is a great way to add high-performance DSP capability to PCI Express-capable systems," said Pierrick Vulliez, CTO of 4DSP. "The FMC sites give designers the ability to select I/O from 4DSP's diverse and growing range of FMC modules as well as from the embedded industry's expanding FMC ecosystem. This flexibility combined with the advanced capabilities of the Kintex UltraScale FPGA and the PC820's serial connectivity options provide a powerful way to design innovative systems with FPGA technology.



Features:

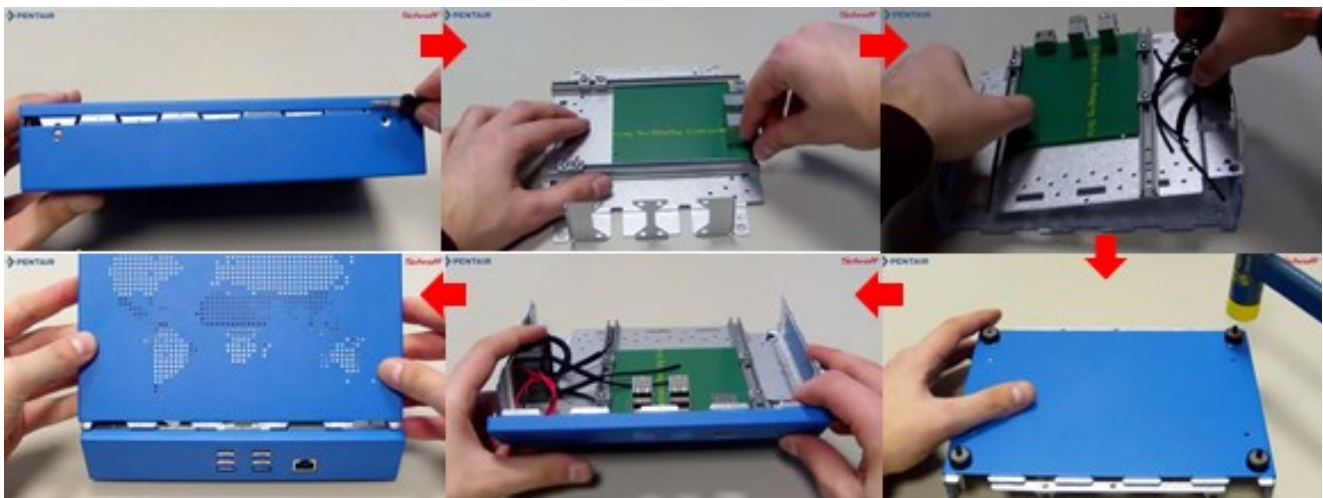
- PCIe Gen3 x8
- 1x Primary FMC HPC (front)
- 1x Secondary FMC HPC (rear)
- 4GB 1600MT/s DDR3 SDRAM
- 256Mb Serial Flash
- Single-lane SFP+ interface
- Bidirectional x2 FireFly connection (14.2 Gbps)
- CPLD on board
- Stand-alone operation (optional)

More details about this product can be found here: <http://www.4dsp.com/pc820.php>

Schroff[®] INTERSCALE M Versatile Enclosures for Small Form Factor boards

For over 50 years Pentair has been a market leader in modular 19" systems with its Schroff brand. With its current launch of the innovative new product 'Interscale M' Pentair now also offers enclosures for non-standardised smaller form factors, so responding with a flexible platform solution to trends such as miniaturisation and individualisation. There are many areas of application for this case: e. g. as a fanless fieldbus enclosure, or for single-board computers or ARM modules, mobile diagnosis or therapeutic equipment for medical systems, PC-based point-of-sale (POS) systems, video monitoring for building services or peripheral control units for industrial applications.

The Interscale M case has a range of special accessories to optimally integrate the electronics according to whether the case is to be used for prototype or production quantities. These include flexible mounting fixtures for PCBs, matching fan kits, and various assembly aids. Visit <http://www.schroff.biz/InterscaleM/> to find out more!



[Click to watch video](#)

ADVANTAGES

- Quick and easy assembly and disassembly with only two screws
- Instant access to electronics
- Shorter integration time thanks to easy plug-in mechanism and optimised accessories
- Integrated EMC protection
- Individual case layout
- Modular off-the-shelf components offer price advantages
- Customisable colour, cut-outs and branding

TECHNICAL CHARACTERISTICS

- 21 standard sizes available from stock with or without side perforation for heat dissipation
- Fine powder-coated finish in RAL 7016; other colours also available
- Sturdy U-shaped body and cover of Al Zn-coated steel
- Aluminium front and rear for easy modification
- 3D STEP data and test reports available to download



Dedicated Systems Australia welcomes Jonathan Knoblauch

Dedicated Systems Australia takes great pleasure in welcoming Jonathan to the team. Jonathan will primarily be working alongside our FPGA customers, providing support and consulting where required.

Name: Jonathan Knoblauch
 Role: Senior Engineer
 Email: jonathan@dedicatedsystems.com.au
 Office: +61 (0)8 8299 9333
 LinkedIn: <http://au.linkedin.com/in/JonathanKnoblauch>



John: Tell me a bit about some places you've worked?

Jonathan: I've worked for larger defence companies like BAE Systems as well as government agency D.S.T.O. My most recent projects involved working with Daronmont and Minelab.

John: How did you end up doing what you do?

Jonathan: I had a keen interest in FPGA development from university and during my time at BAE Systems I bugged my manager to let me work on an FPGA based R&D project that was under development involving radar and UAVs. From there I was hooked and I moved on to more complex FPGA and DSP based projects.

More recently I worked in the field of metal detection with Minelab. It opened my eyes to the values of my earlier physics lectures at Uni and I had the opportunity to become re-acquainted with the different signal and physics processing techniques involved.

John: What excited you about coming to work with the team at Dedicated Systems Australia?

Jonathan: Dedicated Systems partners with leading technology companies. The likes of 4DSP, Bittware, Wind River & RTI work on the cutting edge and its great to see products and hear about new developments in advance. Its also a great place to work. The team comes from quite diverse backgrounds and expertise. There is never a dull moment here, we have a good time.

John: What do you do in your spare time?

Jonathan: In my spare time I like to play music. I sing and play keyboards in a few bands around Adelaide and also like to produce my own music.

Many moons ago, I played in an original band called the New White Sneakers and would like to get back into original band gigs again. I think we might still be on iTunes..

I also have a keen interest in the study and application of Artificial Intelligence.

John: Best gadget of all time?

Jonathan: Nord Stage (Keyboard). It's red so it goes faster.

John: Favourite movie or band?

Jonathan: Favourite Movie : Fight Club
 Favourite Band : Tough question! Lamb / Foo Fighters / Muse



Webinar: Architecting Radar Systems for Flexibility and Reduced Life-Cycle costs

With a rapidly changing threat environment, the need for modern radar systems to keep up and adapt to new technologies under a constrained budget is critical. How do you architect your future radar systems to meet these challenging requirements?

Two different approaches allow new capabilities to be integrated as needed into a scalable, open system:

- Approach 1: Integrate multiple functions – search, tracking, fire control, jamming and other capabilities – into a single standards-based radar system. The open system architecture provides a plug-and-play platform that enables the use of devices and subsystems from multiple vendors. It also reduces redundancy by sharing common processing tasks across systems.
- Approach 2: Network simple sensors and systems together. The linked platforms share data in real time using open standards. It also enables operational capabilities that standalone systems lack.

In this webinar, learn how standards-based communications technologies can be used to architect your future radar systems. See how proven examples of open architectures in radar and combat systems for organisations such as the US Navy have improved flexibility and reduced risk and life cycle costs.

[View Webinar](#)



OpenCL Developer's Bundle - Stratix V FPGA-based PCIe Board and Development Tools for OpenCL

BittWare's OpenCL Developer's Bundle provides the tools necessary to begin developing applications for the Altera Stratix V using OpenCL. OpenCL dramatically simplifies FPGA development by enabling designers to code their systems and algorithms in a high-level C-based framework, directly generating FPGA programming files from a pure software development flow.

The OpenCL Developer's Bundle includes BittWare's S5-PCIe-HQ (S5PH-Q) half-length PCIe board, the BittWorks II system development software, the Altera Quartus II software, and the Altera SDK for OpenCL. This development bundle gives developers access to the latest generation of high-performance FPGAs on a validated COTS PCI Express board, while also significantly reducing their time-to-market by using OpenCL to develop their application.

S5PH-Q PCIe Board

BittWare's S5PH-Q is a Gen3, x8 half-size PCIe card based on the high-bandwidth, power-efficient Altera Stratix V FPGA. The S5PH-Q is a versatile and efficient solution for high-performance network processing, signal processing, and data acquisition, with up to 16 GBytes of on-board DDR3 SDRAM and optional QDRII/II+ up to 72 MB (@ 550 MHz). I/O interfaces include two front-panel QSFP+ cages for serial I/O, two SATA connectors, and timestamping support, as well as RS-232, JTAG, and USB for debug.



- BittWare S5PH-Q Altera Stratix V half-length PCIe board
 - * Stratix V GXA7, GXAB, GSD5, or GSD8
 - * Two banks of 4 GByte DDR3
 - * Four banks of QDRII+ SRAM (optional)
 - * Two QSFP+ cages for 40GbE, 10 GbE, or Infiniband
- S5PH-Q Board Support Package
- BittWare BittWorks II Toolkit system development software for BittWare COTS boards
- Altera Quartus® II software
- Altera Software Development Kit (SDK) for OpenCL

To find out more, [Click Here!](#)



Introducing the New MIL-DNx Series DAQ and I/O Control Platforms



Designed for MIL-STD-461/810/1275 Compliance

UEP's new **DNA-MIL** and **DNR-MIL** platforms are perfect for environmentally harsh I/O acquisition and control applications. Rugged chassis constructions make the DNA-MIL and DNR-MIL perfect for the toughest military and aerospace deployments, as well as challenging I/O applications such as oil drilling platforms and refineries, liquid and gas storage tanks, heavy machinery, and outdoor test stands.

Configurable COTS solutions

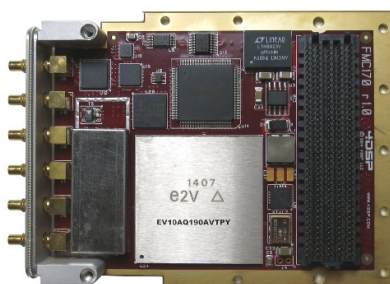
The DNx-MIL platforms are 100% COTS and highly modular to support any analog/digital, interface/sensor, input/output. With over 50 plug-in compatible analog and digital I/O boards from which to choose, either platform can be customised for functionality and optimised for performance.



4DSP Breaks New Barrier in FMC Form Factor with 2.5Ghz Instantaneous Analog Bandwidth Solution

4DSP announces the release of a new analog-to-digital (A/D) / digital-to-analog (D/A) FPGA Mezzanine Card (FMC) card for single-channel data acquisition and high-speed signal processing and recording. The **FMC170** is an FMC daughter card that provides one 10-bit A/D channel with speeds up to 5 Gsps and one 10-bit D/A channel at 5 Gsps. It offers front panel analog I/O access and can be used in a conduction-cooled environment. This module delivers high-bandwidth connectivity for calculation-heavy FPGA-based applications. The FMC170 is very well-suited for high performance applications in the communications, medical, and defence industries.

The low latency data path of the FMC170 enables 2.5GHz of instantaneous bandwidth in both the receive and transmit directions. The analog signal input and output are AC-coupled and connected to MMCX or SSMC coax connectors on the front panel. The FMC170 allows flexible control of clock source, sampling frequency, and calibration through I2C communication. The FMC170 is ideal for the high data throughput requirements of RADAR/SONAR and aerospace



Features:

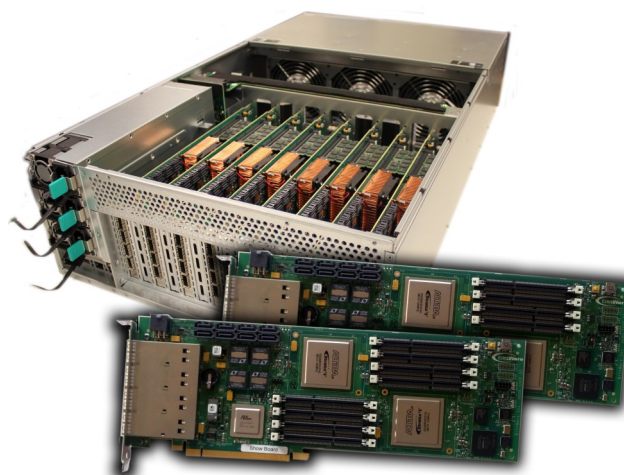
- Single-channel, 10-bit A/D up to 5Gsps
- Single-channel, 10-bit D/A up to 5Gsps
- VITA 57.1-2010 compliant
- Conduction-cooled - Standard Option
- AC-coupled analog signals
- LVDS IO signalling
- 6 SSMC or MMCX front panel connectors
- Clock source, sampling frequency, and calibration through I2C communication
- Flexible clock tree enables:
 - * Internal clock source
 - * External sampling or reference clock
- Power-down modes to switch off unused functions for system power savings
- Mil-I-46058c Conformal Coating Compliant (optional)
- HPC - High Pin Count connector



TeraBox High Performance Reconfigurable Computing Platform

BittWare's **TeraBox** is an ultra high-performance FPGA platform ideal for network/packet processing and high performance computing (HPC) applications. Featuring up to sixteen of the largest Altera Arria® 10 or Stratix® V Family FPGAs, the TeraBox offers 24 TeraFLOPS of processing power, along with 6.5 Terabits/sec of memory bandwidth and 1.28 Terabits/sec of I/O – all in a turnkey rackmount solution. The system arrives tested and configured, and includes complete development software support with **BittWare's BittWorks II Toolkit**, allowing users to immediately focus on developing their specific application.

- 24 TeraFLOPS processing: 16x Altera Arria 10 or Stratix V FPGAs
 - * Up to 18 million logic elements (Arria 10 GX)
 - * Up to 62,000 multipliers (Stratix V GS)
- 4U or 5U Rackmount PCIe system (server, industrial, or expansion)
 - * Dual socket Intel Ivy Bridge with up to 12 cores
 - * Up to 768 GBytes of system memory
 - * 8 Gen3 x16 PCIe slots
- Complete software support
 - * Windows and Linux 64 drivers, interface libraries, and hardware management
 - * FPGA development kit for Arria 10 and Stratix V



- 1.28 Terabits/sec I/O
 - * 128x 10GigE, 32x 40GigE, 32x 100 GigE, or 32x QDR Infiniband
- 6.5 Terabits/sec memory bandwidth
 - * Up to 64 banks DDR3-1600 (512 GBytes)
 - * DDR4, QDR-IV, QDRII+, and RLD RAM3 memory options

BittWare Arria 10 and Stratix V FPGA PCIe Boards

BittWare's PCIe board platforms offer extremely flexible memory configuration options, with SO-DIMM sites supporting DDR4 SDRAM, DDR3 SDRAM, QDR-IV, QDRII+, or RLD RAM3. For example, with its eight SO-DIMM sites populated, the Stratix V based S5PE-DS supports up to 64 GBytes of DDR3-1600 SDRAM, for a system total of 512 GBytes in 64 banks, with 6.5 Terabits/sec of memory bandwidth.

The boards offer up to 4 QSFP+ cages, each supporting 40GigE, 4x 10GigE, or QDR/FDR InfiniBand interfaces direct to the FPGAs' built-in PHYs for the lowest possible latency. Arria 10 boards also support 100GigE. The QSFPs can be used to interconnect the boards and multiple TeraBox platforms to make bigger clusters, making it ideal for HPC applications, while the low latency 10GigE and 40GigE interfaces are ideal for packet processing.

4U or 5U PCIe Rackmount Chassis

The TeraBox supports three chassis options: a 4U server, a 5U industrial PC, or a 5U PCIe expansion system. The server-based system features a rackmount chassis including dual Intel Ivy Bridge processors with up to 12 cores, 768 GBytes of system memory, and 8 Gen3 x16 PCIe slots. The 5U industrial system features a rackmount chassis including a 3.4 GHz Xeon SBC. The expansion system option features a PCIe Gen2 expansion system with eight double-width x16 slots and 80 Gbit/sec host bus-to-expansion system bandwidth.

WIND RIVER**Wind River Delivers Accelerated Safety Certification
for Multi-core with New VxWorks Profile**

Wind River®, a world leader in delivering software for intelligent connected systems, has introduced a safety profile for the next-generation version of its VxWorks® real-time operating system (RTOS). The profile adds safety features to VxWorks 7 aimed at development of safety critical systems in industrial, medical, transportation, aerospace, and defense. Additionally, Wind River has enhanced its Virtualization Profile for VxWorks.

The new [Safety Profile for VxWorks](#) delivers advanced time and space partitioning capabilities to ensure reliable, interference-free consolidation of multiple applications with different levels of safety criticality on one hardware platform, single or multi-core. Consolidation helps customers meet stringent safety requirements with a variety of system design options while driving down bill-of-material and maintenance costs. Furthermore, separation of applications of different criticality levels allows customers to update specific applications in a targeted fashion, without having to retest or recertify the entire system.

In addition, the profile has received pre-approval by TÜV SÜD for IEC 61508-3 SIL3 conformance. The optional certification evidence package will help VxWorks customers reduce cost, risk, and time-to-certification for their embedded systems. Safety Profile will also serve as the future foundation that will help customers certify their devices to additional IEC standards.

"With Safety Profile for VxWorks, developers can take full advantage of technological advances in microprocessors that VxWorks enables, with the confidence that they will have a strong OS foundation to meet the most demanding safety certification standards," said Dinyar Dastoor, vice president of product management at Wind River. "For three-plus decades Wind River has been a trusted technology partner to companies in markets where safety and reliability are paramount, and this is just another proof point of our commitment to providing robust safety features across our product portfolio."

Recognised as the industry-leading RTOS, VxWorks boasts a modular, scalable architecture that separates the VxWorks core from middleware, applications, and other packages, enabling bug fixes, upgrades, and new feature additions to be accomplished faster.

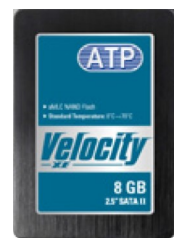
**ATP's aMLC (advancedMLC) for
Embedded Modules and 2.5" SSDs**

Endurance, performance, and data retention are a few critical factors for a NAND Flash storage device to meet the demanding industrial operating requirements. To face these engineering challenges, ATP, a leading manufacturer of embedded Flash and ruggedised SSDs and DRAM modules, has offered a new advanced firmware technology, aMLC, to implement onto ATP's NAND Flash products.

The new ATP aMLC solution provides a less-than-SLC-cost solution in return for a full scale property improvement of advanced Reliability, Density, P/E cycles, Performance with competitive pricing (RDPPP). ATP aMLC product lines include 2.5"SSDs, SlimSATA and mSATA with flexible densities ranging from 8GB~64GB, as more form factors and densities are to be followed. The mainstream densities are best suited for the most up-to-date industrial demands on any write intensive or performance driven applications.

The modern automobile navigates direction, collects data, communicates with vehicles, and even links to other devices to enhance the efficiency of traffic management. Therefore, reliability and long-term data integrity are critical to automotive applications. ATP offers the advanced firmware technology, aMLC, to transfer NAND Flash from four states of MLC to two states. Due to its greater cell disturbance margin and subsequently larger program/erase cycles, overall performance and data retention have greatly improved. For the automotive and other industrial applications, ATP provides the Wide Temperature (WT) DRAM solution, which utilises the IC Level tests and the system level burning in-tests to ensure that the products meet and exceed extreme WT (-40°C to 85°C) operating conditions with industrial grade quality and reliability.

Learn more about aMLC at [ATP Electronics](#)

8G~64G
SlimSATA8G~64G
mSATA8G~64G
2.5" SSD



AdaCore's CodePeer Static Analysis Tool Earns Qualification for Software Verification in Avionics, Railway

AdaCore has announced that its **CodePeer** advanced static analysis tool for the automated review and validation of Ada source code has been qualified as a software verification tool for developers in both avionics and railway industries.

CodePeer assesses the program before execution to find errors efficiently and early in the development life cycle. Using advanced mathematics, CodePeer analyses every line of software, considering every possible input and every path through the program. It performs impact and vulnerability analysis when existing code is modified, and, using control-flow, data-flow and other advanced static analysis techniques, it detects problems that would otherwise require labour-intensive debugging.

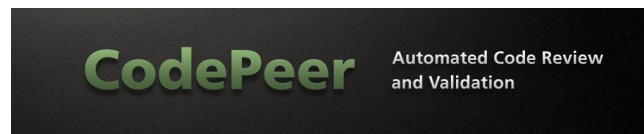
“In safety-critical domains, developers need very strong assurances that the tool they’re using to assess their code is reliable, can be trusted, and will substantially reduce the need for manual code review,” says Arnaud Charlet, CodePeer Product Manager and Technical Director at AdaCore. “CodePeer has been through rigorous industry-specific tests for avionics and railway that fully affirm its value and reliability in these and other safety-critical development environments.”

Avionics Qualification

CodePeer has been qualified as a verification tool for DO-178B, the software safety standard for commercial airborne systems. Certification authorities such as the FAA in the U.S. and EASA in Europe apply DO-178B to provide confidence that the software will meet its requirements.

Vulnerabilities detected by CodePeer analysis for avionics include following:

- Overflow on integer and floating point types
- Range violations on integer and floating point types
- Index violations on array operations
- Division by zero on integer and floating point types
- Uninitialised variables
- Underflow on floating point types



Where no potential error is reported, CodePeer guarantees that the code is exempt from these vulnerabilities.

Railway Qualification

For railway applications, CodePeer has been used to verify code certified in accordance with CENELEC EN 50128:2011 SIL 4 --the highest safety integrity level.

In this context, CodePeer has been used for the following activities:

- Boundary value analysis: it detects attempts to dereference a pointer that could be null, to read values outside the bounds of an Ada type or subtype, and also detects buffer overflows, numeric overflow or wraparound, and division by zero.
- Control flow analysis: it detects suspicious and potentially incorrect control flows, such as unreachable code, redundant conditionals, loops that either run forever or fail to terminate normally, and subprograms that never return.
- Data flow analysis: it detects suspicious and potentially incorrect data flows, such as variables read before they are written (uninitialised variables), variables written more than once without being read (redundant assignments), variables that are written but never read, and parameters with an incorrect mode (unread parameter, unassigned parameter).

CodePeer can be used in conjunction with AdaCore's GNAT Pro development environment where it is tightly integrated into AdaCore's GPS (GNAT Programming Studio) and GNATbench IDEs, or as a standalone product. It comes with a number of complementary static analysis tools common to the technology: a coding standard verification tool (GNATcheck), a source code metric generator (GNATmetric), a semantic analyser and a document generator.