Dedicated Systems' News

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Front Removable VME and CPCI Storage Boards

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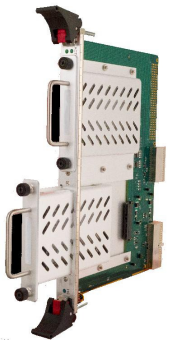
The boards are 6U SATA storage modules with dual front removable storage drives. They are configured to provide SATA I/O for dual 2.5" drives using a rear transition module or break out board via the CPCI J3 or VME P0 connectors. Each single drive can be removed independently for easy system upgrade, data transport or drive replacement. The boards may be utilised singularly or integrated as part of a multi-slot storage array using an external SATA RAID controller.

Features and Benefits:



- Choose the latest in solid state drive technology (SLC, MLC or eMLC) or standard, enhanced or extended duty rotating drives
- Supports current drive capacities currently over 2TB per board
- 3Gb data rates are supported
- Standard 6U x 4HP x160mm form factor
- Drive Activity LEDs
- Individual drive shuttles are front removable, not hot pluggable
- Optional Rear Transition Module (RTM) providing SATA port connectivity from the rear
- RoHS compliant and lead free

- High data rates for current application needs
- Addresses high capacity storage needs
- Capable of providing RAID 0, 1 or 5 via software RAID
- Easy system upgrade, data transport or maintenance with front removability
- Operates in temperature extremes to -40C to +85C using solid-state drives
- Multi-slot expansion capability enables high capacity array design

Top Five Webinars of 2012

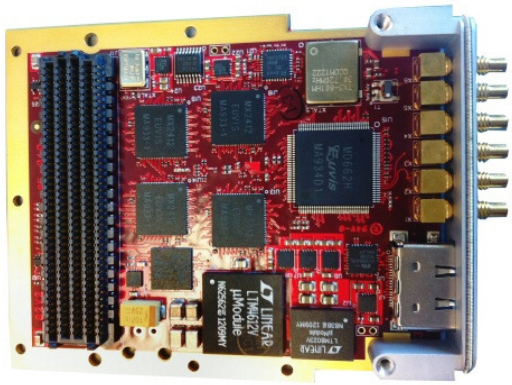
- **The Promise of Interoperable Open Architecture** - Dive into the motivations, standards, technologies, and business models that drive the OA movement
- **Open Source 2.0?** - Discover the business factors driving open source and the rationale and benefits behind RTI's new Open Community Source licensing and business model
- **Don't Architect a Real-Time System that Can't Scale** - Look into how you can apply proven integration techniques – such as loose coupling and service orientation – to demanding real-time systems
- **The Single Most Important Decision in Designing Your Distributed System** - Examine whether to go with the message-centric or data-centric approach in designing your distributed system
- **Top Ten Ways to Mess Up Your Distributed System** - Avoid commonly made mistakes when designing your distributed system

Did you miss them? Watch the on-demand replays starting from here: http://www.rti.com/mk/webinars.html

New FMC Modules from 4DSP

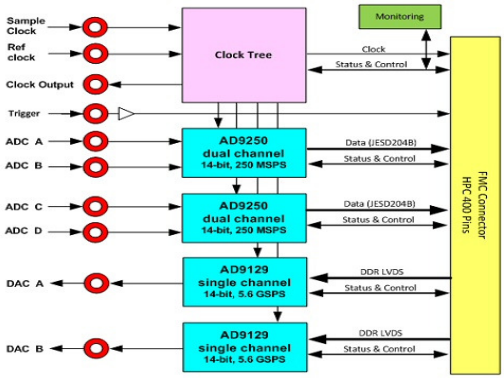
FMC210 -HPC Digital-to-Analog Converter Board
One Channel 10-bit D/A @ 8000 Msps

- Single channel 10-bit 8Gsps D/A conversion
- VITA 57.1-2010 compliant
- Conduction Cooled - Standard Option
- LVDS IO signalling
- Differential DC-coupled analog output
- Clock Source and Sampling Frequency through I2C
- Flexible clock tree enables
  - internal sampling clock
  - external reference and sampling clock
- HPC - High Pin Count Connector
- Front panel SSMC connectors
- Power-down modes to switch off unused functions for system power savings
- Mil-I-46058c Conformal Coating Optional



FMC176 – HPC D/A and A/D Module
Quad 14-bit 250Msps A/D - Dual 14-bit 5.6Gsps D/A

- Two **AD9250**: 4-channel 14-bit A/D up to 250 Msps
- Two **AD9129**: 2-channel 14-bit D/A up to 5.6 Gsps (2.8Gsps without 1:2 interpolation) - LVDS
- VITA 57.1-2010 compliant
- Conduction Cooled – Standard Option
- Single ended AC-coupled analog signals.
- 10 MMCX/SSMC connectors available from the front panel
- Clock Source, Sampling Frequency, and Calibration through SPI communication busses
- Flexible clock tree enables:
  - internal clock source, external reference clock, external sampling clock
- Power-down modes to switch off unused functions
- Mil-I-46058c Conformal Coating Optional



GNAT Pro solves Data Endianness Portability Challenge

Automatically handles conversions, simplifies Ada development and maintenance

AdaCore announced the implementation of a new GNAT Pro feature that allows Ada developers to portably and reliably define data layout in an endianness-independent fashion. This capability makes it possible to port and reuse existing code bases on a different hardware platform, without having to manually implement the error-prone, byte-swapping logic that would otherwise be needed.

Portability is a key requirement for many Ada applications, which often have to be maintained and perhaps augmented with new functionality, over a time-span comprising many years. Their lifetime often survives major evolutions in hardware architecture, moving away from old platforms either for obsolescence reasons or because of costs. Whatever the reason, x86 platforms are now typical targets for many projects. However, the x86 processor represents numeric data in 'little endian' format (lower address for lower order byte), while legacy platforms, such as 68K, PowerPC, and SPARC, are in 'big endian' format (lower address for higher order byte). This difference can make the porting effort a substantial and error-prone endeavour, and, indeed, the costs and risks associated with moving to a different binary representation may simply be prohibitive.

To solve this problem, GNAT Pro has introduced an 'endianness-agnostic' enhancement to specify the endianness of a specific data structure independent of the underlying architecture. The definition of the representation uses a natural extension to the existing Ada data representation model. Ada source code is thus portable across big endian and little endian architectures, even when manipulating low-level data structure representations. The cumbersome and error-prone task of writing bitwise data manipulation is transparently managed by the compiler, significantly simplifying the task of porting such applications between architectures.

WIND RIVER

NASA relies on Wind River Simulation Technology for Long-Term Cost Savings

Wind River, a world leader in embedded and mobile software, has announced that NASA's Independent Verification and Validation (IV&V) Program is using **Wind River Simics**, a full system simulator, for its high-fidelity simulator product, GO-SIM.

NASA's IV&V Program was founded as part of NASA's strategy to provide the highest achievable levels of safety and cost-effectiveness for mission-critical software. Because its primary business includes software test and verification, software simulations are an essential part of the business. For this reason, Simics has become an important component of NASA's IV&V group's GO-SIM product. GO-SIM's functions include loading and running unmodified flight software binaries, executing flight scripts, performing single-step debugging, injecting errors via the ground system, stressing the system under test, and validating findings from other analyses.

Simics enables target software to run on a virtual platform the same way it does on physical hardware. Along with Simics' capabilities of scripting, debugging, inspection and fault injection, it enables users to define, develop and integrate their systems without the constraints of physical target hardware. Simics allowed NASA's IV&V team to simulate their target hardware, ranging from a single processor to large, complex, and connected electronic systems, and build its GO-SIM product with all the desired features.

"It is gratifying to know that Wind River has enabled the NASA IV&V group to successfully meet its goals to develop a complete simulator in a reduced time frame and at a lower cost than if it had performed traditional hardware simulations," said Michel Genard, vice president of tools and lifecycle solutions at Wind River. "In addition to minimizing target hardware dependencies by using Simics, 80—90% of the simulation models created can be reused for other missions, representing tremendous long-term cost savings for NASA."

EKF SYSTEM

SC1 - CompactPCI ® Serial SBC

Intel® Core™ i7-3xxx Processor

EKF has introduced the first native CompactPCI® Serial CPU board. The SC1-ALLEGRO is a rich featured high performance 4HP/3U system controller, equipped with a 3rd generation Intel® Core™mobile processor (i7 Ivy Bridge + ECC). The SC1-ALLEGRO front panel is provided with two Gigabit Ethernet jacks, two USB 3.0 receptacles, and two Mini-DisplayPort connectors for attachment of high resolution digital displays. The SC1-ALLEGRO is equipped with up to 16GB RAM with ECC support. 8GB memory-down are provided for rugged applications, and another 8GB are available via the DDR3 ECC SO-DIMM socket. As an option, a low profile mezzanine module with dual mSATA SSDs may serve as a high-speed RAID mass storage solution. The SC1-ALLEGRO backplane connectors comply with the PICMG® CompactPCI® Serial system slot specification.

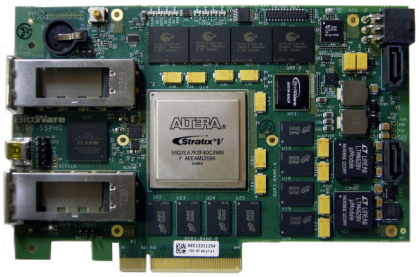
While mechanically compliant to CompactPCI® Classic, CompactPCI® Serial (PICMG® CPCIS.0) defines a completely new card slot, based on PCI Express®, SATA, Gigabit Ethernet and USB serial data lines. Up to 6 high-speed backplane connectors P1 - P6 are provided on a system slot controller such as the SC1-ALLEGRO, which can be considered as a root hub with respect to most signal lines. A passive backplane is used for distribution of a defined subset of I/O channels from the system slot to each of up to eight peripheral slots in a CompactPCI® Serial system.

Most CompactPCI® Serial peripheral slot cards require only the backplane connector P1, which comprises PCIe, SATA and USB signals, resulting in a concise and inexpensive peripheral board design. More powerful peripheral cards profit from so called Fat Pipe slots (PCIe x 8). The SC1-ALLEGRO is a native CompactPCI® Serial CPU card, suitable for usage in a pure CPCI Serial environment. Due to its generous backplane capabilities (20 x PCI Express® lanes, 6 x USB, 6 x SATA RAID, 2 x GbE), very powerful industrial systems can be built.

Special Pricing for Altera Stratix® V FPGA PCIe Board for OpenCL Development

BittWare has announced that their **S5-PCIe-HQ (S5PH-Q) PCIe** COTS board populated with the Altera Stratix V GSMD5 device has been specially priced for use with Altera's Software Development Kit (SDK) for OpenCL. The S5PH-Q is a half-length PCIe card based on Altera's high-performance 28-nm Stratix V FPGAs, providing a versatile and efficient solution for high-performance network processing, signal processing, and data acquisition. **The S5PH-Q GSMD5 is available now for Altera OpenCL Early Access Program (EAP) customers**, along with BittWare's BittWorks II Toolkit and Altera's SDK for OpenCL, creating an ideal platform for Stratix V-based OpenCL development. Future Altera SDK support for BittWare's S5PH-Q will include both the Altera Stratix V GSMD8 and GXMA7 devices.

Benefits of OpenCL for FPGAs:



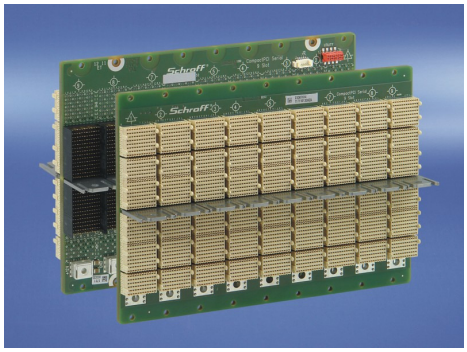
- Faster time-to-market using the OpenCL C-based parallel programming language as opposed to low-level hardware description language (HDL).
- Quick design exploration by working at a higher level of design abstraction.
- Easy design re-use by re-targeting existing OpenCL C code to current and future FPGAs.
- Faster design completion by generating an FPGA implementation of OpenCL C code in a single step, bypassing the manual timing closure efforts and implementation of communication interfaces between the FPGA, host, and external memories.
- Increased performance by offloading performance-intensive functions from the host processor to the FPGA
- Significantly lower power by using the Altera SDK for OpenCL which generates only the logic needed to deliver the required application

BittWare's OpenCL Development Support includes:

- BittWare **S5-PCI-HQ** Altera Stratix V GSMD5 half-length PCIe board with two banks of 4GByte DDR3 SDRAM
- BittWare BittWorks II Toolkit application development software for BittWare COTS boards
- BittWare Breakout Board (BWBO) providing front panel access to signals and interfaces on the S5PH-Q (two RS-232 connectors, an RJ-45 Ethernet jack, and a micro-USB shell that are all accessible via the front panel)
- Altera Quartus® II software
- Altera SDK for OpenCL available from Altera for their OpenCL EAP customers
- Altera USB Byte Blaster to download configuration or program data into the Stratix V

CompactPCI ® Serial Backplanes

CompactPCI Serial is a new standard supporting the fast serial protocols PCI Express, SATA, USB and Ethernet. Schroff backplanes already support the next generation of protocols (PCIe up to Gen3, SATA up to rev. 3.0, USB 2.0 & 3.0 and Ethernet up to 10G Base-T). All 4 protocols are available simultaneously on each slot .



A maximum number of 9 slots are possible (one system slot and up to 8 peripheral slots). A robust coding pin in stainless steel allows use even in harsh environments.

Backplanes are available with Full Mesh or Single-Star Ethernet (see graph) topologies, with or without Rear I/O .

Chassis and power supplies are available in many sizes and configurations.